REMARKS

Reconsideration of the application as amended herein is respectfully requested. By this Amendment and response, claims 1, 2-5 and 7 have been cancelled. Claims 2, 8, 9-10 have been amended and claims 11-13 have been added. Thus, claims 2,6, 8-13 remain.

Specification

The Office Action has objected the abstract of disclosure because the abstract exceeds 150 words in length. Applicant has amended the abstract so as to overcome this objection.

Drawings

The Office Action has objected the drawings as failing to comply with 37 CFR 1.84(p)(5). Applicant is submitting herewith corrected drawings, which are attached hereto as Exhibit A.

Claim Objection

The Office Action has objected claims 1-7 and 9 because of informalities. Claim 1 has been cancelled, thereby rendering this objection moot. Applicant has amended claim 9 in such a manner that overcomes this objection.

Rejections Under 35 U.S.C. § 102

The Office Action has rejected claims 2, 6 and 8 under 35 U.S.C. § 102(e) as being anticipated by Maruyama (US 6205567 B1). Applicant respectfully traverses this rejection. Regarding claim 2, the Office Action states that col. 9, lines 37-45 in Maruyama teaches "backtracing from each observable node, said backtrace through each of said internal nodes

being based on said fault-free circuit simulation". Applicant respectfully disagrees. Maruyama teaches that "back tracing" is as follows:

> "Forward Circuit Area": an area including all combinational circuits which can be traced through *back tracing* started from input pins of the storage element to scan-in points or primary input terminals (see FIG. 8).
> "Backward Circuit Area": an area including all combinational circuits which can be traced through *back tracing* started from scan-out points or primary output terminals to the output pins of the storage element, the scan points, and the primary input terminals (see FIG. 8). (emphasis added)

Thus, the "back tracing" discussion in Maruyama is used to help explain what is meant by the terms "forward circuit area" and "backward circuit area" in Explanation of Terminology portion of Maruyama (col. 9, line 24). The "forward circuit area" and "backward circuit area" are used to describe the invention disclosed by Maruyama (See e.g., Abstract, lines 5-17):

> In the fault simulation method, the integrated circuit is divided into a *backward circuit area*, which is a combinational circuit area on the output-pin side of a storage element included in the integrated circuit, and a *forward circuit area*, which is a combinational circuit area on the input-pin side of the storage element. When a fault which propagates to input pins of the storage element exists in the forward circuit area, the value of the fault at that observation time is written into the storage element, and at a later observation time the value of the fault is read from the storage element and propagated to the backward circuit area from output pins of the storage element. (emphasis added)

In short, the "back tracing" taught by Maruyama is not a step of the actual fault simulation method disclosed therein. Indeed, Maruyama does not describe "back tracing" in "[1] Description of the Configuration of the Fault Simulation Apparatus" (col. 10, line 48) or anywhere else where the fault simulation of Maruyama is described. In addition, Maruyama does not have a statement that associates the "back tracing" with "good machine simulation" (or

fault-free circuit simulation). In other words, Maruyama does not teach that "back tracing" is based on said "good machine simulation" as required by claim 2.

The Office Action also states that Maruyama teaches that backtracing through each of the internal nodes is "limited to paths along which a faulty value has a possibility of propagating to said observable node". The Office Action argues that this is taught at col. 5, lines 5-14 ("Maruyama teach only paths capable of propagating a faulty value to said observable node are activated"). Applicant respectfully disagrees. The cited part of Maruyama actually says:

> In the fault simulation method, the writing of data into the storage element is monitored at the time of the true-value simulation. When the writing of data into the storage element--to which a fault is propagated from the forward circuit area at certain observation time--is detected during true-value simulation, the value of the fault is stored, and the value of the fault is read at a later observation time and is propagated to the backward circuit area from the output pins of the storage element.

This citation does not say anything about a "path". Regardless, even if this citation teaches a "path", Maruyama still does not teach that "back tracing" is limited to the "path". This is natural consequence since Maruyama does not describe the step of "back tracing" itself, as mentioned above. Consequently, the subject matter of claim 2 is patentably distinguishable from Maruyama. Based on this, Applicant respectfully submits that claim 2 is in condition for allowance, which is respectfully requested.

Claim 6 is allowable because it is dependent on claim 2, which is allowable.

Applicant has amended claim 8 such that the arguments relating to claim 2 are equally applicable to claim 8. Based on this, Applicant respectfully submits that claim 8 is in condition for allowance, which is respectfully requested.

Rejections Under 35 U.S.C. § 103

The Office Action has rejected claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Maruyama (US 6205567 B1). Applicant respectfully traverses this rejection. Applicant has amended claims 9 and 10 such that the same arguments regarding claim 2 apply to claims 9 and 10. Based on this, Applicant respectfully submits that claims 9 and 10 are in condition for allowance, which is respectfully requested.

Based on the foregoing, Applicant respectfully submits that this application is in condition for allowance, which is respectfully requested.

Should the Examiner have any questions or comments on the application, the Examiner should feel free to contact the undersigned via telephone.

Respectfully submitted,
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